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(54) **Column multiplexer**

Spaltenmultiplexer

Multiplexeur de colonne

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## Description

**[0001]** The present invention relates to high integration EPROM, FLASH-EPROM, ROM and DRAM memories and more in particular to an improved architecture of the multiplexer of column selection (COLUMN MUX).

**[0002]** The decoding circuitry allows the access, during the reading or writing phase, to the cell identified by a certain address fed to the relative inputs of the memory. During a reading phase to each bit of the output data (word) corresponds a selected cell. Commonly, upon row selection a row of cells is switched on, whereas, upon column decoding, it is selected which output bit line (column) is coupled to a bit sensing node.

**[0003]** In high integration, state-of-the-art, EPROM, FLASH-EPROM, ROM or DRAM memories and so forth, wherein each elementary cell occupies an area of a few square micrometers, the decoding circuitry represents a critical item of the design, because it must satisfy more and more stringent requisites of compactness, speed and low power consumption.

**[0004]** The realization of a column multiplexer in higher and higher scale of integration devices is known to imply difficulties because of the reduced dimensions of the cells. Each new (technological) generation of these devices exasperates and aggravates these problem. Usually these difficulties imply the following:

- area requisite always to the limit of implementation;
- accentuation of associated parasitic electrical parameters;
- decline of efficiency in terms if reduced multiplexer speed;
- inevitable criticality of some structures.

**[0005]** According to EP 0 312 738 isolation between N+ diffused regions belonging to adjacent active devices of an integrated circuit is provided by forming an isolating transistor sharing the adjacent N+ regions and with a gate electrode of a polysilicon of the same conductivity type as the underlying semiconductor region between said $N^+$ regions for increasing the threshold voltage of the isolating transistor and biasing it to ground potential.

**[0006]** One of the constraints that are most responsible for the above mentioned difficulties in finding the area in which the column multiplexer may be realized is compliance with the minimum isolation distance between adjacent diffusions which, in present fabrication processes may be of about 1.8μm.

**[0007]** This minimum distance is relatively large if compared to matrix cells dimensions that in this type of processes may be of 1.7μm*1.7μm.

**[0008]** The repetitive electric scheme of a column multiplexer is depicted in Figure 1.

**[0009]** With reference to the constraints of a fabrication process according to state-of-the-art technology, the minimum distance of separation between two adjacent diffusions of the devices making up the multiplexer (in conformity with the circuital scheme of Figure 1), may be represented, respectively in a plan view and in a cross-section, as shown in Figures 4 and 5. Indicatively, in the plan view of Figure 4 is highlighted the minimum distance requisite that a contact area must have from the edge of the diffusion, which in this kind of processes may be of 0.2μm.

**[0010]** On the other hand, the relative compactness of a matrix having a linewidth of just about 1.7μm compels, for obvious dimensional limitations, to a reduction of the depth of the diffusions and proportionally to an increase of their length in order to ensure a correct functioning of the integrated devices, as well as limiting the frequency (number) of equipotentiality contacts. This leads to the realization of a particularly resistive and capacitive column multiplexer structure, that is geometric constraints cause a considerable increment of the "parasitive" electrical parameters associated to the integrated structure of the multiplexer that reduces the efficiency in terms of an increase of the time constants.

**[0011]** Moreover, the layout tends to became highly "tortuous" because of the fragmentation of the active areas and "burdensome" for the accompanying problems that such an "tortuous" layout raises in realizing the electric paths to the control terminals and their "multiplexing", for sake of equipotentiality.

**[0012]** Confronted with these drawbacks and constraints, it has now been found, and this is the object of the present invention, a more efficient column multiplexer architecture than the comparable architectures used nowadays. In practice, the architecture of the invention allows for a decisive relaxation of the minimum isolation distance constraint between adjacent diffusions in designing the layout of a column multiplexer.

**[0013]** Primarily, the invention is based upon the realization of an isolating transistor in place of the inter-diffusion separation space, typical of layouts of known column multiplexers.

**[0014]** Instead, by realizing an isolating transistor, or in practice an isolating gate, short-circuited to ground, a dimensional saving in the order of 1.05μm may be attained, considering that the total separating distance between two adjacent contacts used to be of about 2.20μm for the case depicted in Figure 2.

**[0015]** Considering that the column multiplexing is usually arranged by relatively small modules, that is by bunches of a relatively small number of bitlines, for example of 16 bitlines (columns) plus a ground line (GND), according to a particularly preferred embodiment of the multiplexer of the invention, the unitary multiplexer structure (module) is realized in the space in front of two bunches, instead of being opposite to a single one, that is opposite to 16*2 bitlines terminations plus two ground lines.

**[0016]** Moreover, the bitlines relative to two adjacent minimum modules of 16 bitlines each, are interleaved among each other. In this manner, the multiplexer of the

invention is, in terms of the layout, realized on two parallel strips, the multiplexing structure of a first minimum module (bunch) of 16 bitlines being realized on a first strip whereas, the multiplexing structure of the other bunch of 16 bitlines is realized unit on the other strip, parallel to the first In this way, the multiplexing structure relative to a single minimum bunch or module of bit lines is realized on the same strip, in a continuous manner, rather than in a typical offset manner due to space limitation, as normally done nowadays. These considerations will be illustrated in more details here-in-below.

**[0017]** The improved column multiplexer architecture of the invention, besides relieving the above stated geometric constraints, also attains a number of distinguishable advantages that may be summarized as follows:

- it allows a beneficial increase of the diffusion areas of the devices that constitute the column multiplexer, thus improving contacability of the different regions and a reduction of parasitic resistances;
- it permits reduction of the parasitic edge capacitances (reduced length of the boundary towards the field oxide);
- continuity of the two active area region simplifies remarkably the layout;
- the architecture is unconstrained from traditional geometric limitations and lends itself optimally to a further "scaling" in future;
- relaxation of dimensional constraints also offers the possibility of increasing the size of the transistors that made up the multiplexer and this may constitute an important aspect in improving the memory performances during reading programming phases.

**Figure 1**, as already mentioned above, is an repetitive electric scheme of a typical column multiplexer;
**Figure 2** highlights the parasitic elements (resistive and capacitive) of the integrated architecture of column multiplexer of Figure 1, accentuated by existing dimensional constraints;
**Figure 3** is a repetitive electric scheme of a module of column multiplexer according to the architecture of this invention;
**Figures 4 and 5**, as already mentioned above illustrate on a plan view and on a cross-section, respectively, certain layout restraints between adjacently integrated devices of a column multiplexer according to the scheme shown in Figure 1;
**Figures 6 and 7** highlight the exceptional relaxation of the dimensional limitations, compared to the known architecture of Figures 4 and 5;
**Figures 8 and 9** are partial layout views that compare the constraints and critical ties of a known layout with those of a layout of the present invention.
As shown in Figures 1 and 2, the basic or modular electric scheme of a column multiplexer may be described as consisting of a row of select transistors M0, M1, M2, M3,...,M14, M15,... .Each transistor has its own current terminals connected respectively to a bitline (BL0, BL1,...,BL14,BL15,...) and to an output common node OUT of the multiplexer module.

**[0018]** Taking into consideration the integrated structure of the multiplexer circuit, it can be noticed that between two adjacent diffusions, belonging to two distinct transistors of two adjacent pairs, that is between the coupling nodes of respective current terminals to two adjacent bitlines in a normal memory layout, a certain minimum separating distance must be maintained to ensure an adequate isolation between the two diffusions that, during the functioning of the multiplexer, may assume quite different potentials (0 and VCC).

**[0019]** Such constraints of minimum distance of inter-diffusion separation are brought to the fore in the plan view of Figure 4 and in the cross-section of Figure 5, in which A identifies the diffusion of a transistor and B the diffusion of an adjacent transistor, belonging to a different pair of transistors. In Figure 4 is also highlighted another dimensional limitation represented by the need of ensuring a minimum distance between the area of a contact C (for the connection to the respective bitline) and the edge of the diffusion.

**[0020]** These dimensional costraints contrast with the limited space available because of the compactness (narrowness of the definition line width) of modern memory cell arrays, obliging to a reduction of the width of the transistor diffusions and to a proportional elongation thereof to the extent needed to ensure a sufficient diffusion area.

**[0021]** In memories of a high degree of integration, these layout constraints and dimensional compromises have negative repercussions by enhancing parasitic, resistive and capacitive electric parameters, symbolically so pointed out in the electric scheme of Figure 2.

**[0022]** Figure 3 shows the circuit diagram of a column multiplexer circuit realized according to the present invention.

**[0023]** The diagram depicts a multiplexer module handling 16 bitlines (BL0, BL1, BL2, BL3,...,BL14, BL15).

**[0024]** According to the architecture of the invention, the isolation amongst the connection nodes of each bitline to the respective select transistor of the multiplexer circuit, is ensured by an isolating transistor, namely (Mi0, Mi1, Mi3,...,Mi13,Mi14.

**[0025]** The integration manner of the architecture of the invention, comparable with an architecture of the prior art as shown in Figures 4 and 5, is depicted in Figures 6 and 7, defining a plan view and cross-section view, respectively.

**[0026]** In practice, the column multiplexer circuit of the invention achieves a reduction of more than one micrometer for each isolation point along the width direction as highlighted in the cross-sections of Figures 5 and

7.

**[0027]** The advantages of the invention will be more evident by comparing a typical layout according to a common arrangement of a column multiplexer as shown in Figure 8, with a layout realized according to the present invention, as shown in Figure 9.

**[0028]** In this important example of an embodiment of the invention, the increased compactness provided by the architecture of the invention is exploited, rather than for realizing an exasperated saving of silicon area, which, depending on the particular architecture of the memory array, may not be in itself a fundamental requisite, because often column multiplexers are realized in spaces that are made available by the general layout of the architectural blocks that made up the array, but rather for relaxing certain minimum distance requisites, to favor a "distributed" contacting with the aim of reducing ohmic contributions, to eliminate critical aspects of the process as well as to produce a more "streamlined" layout, that is less "tortuous".

**[0029]** With reference to Figure 8, where a layout according to current fabrication techniques is shown, the column selection multiplexer for a certain number or bunch of (32) bitlines, BL_0<0-15> and BL_1<0-15>, is organized by forming the necessary 8+8 select transistors in two rows or orders, because of a general layout constrint, since the minimum "pitch" (distance of separation) between two adjacent select transistors would not be compliant with the bitlines "pitch".

**[0030]** Therefore, alternately by pairs, the bitlines are prolonged through the space between two select transistors of a first or front row or order to the respective select transistors of the second or back row or order of transistors.

**[0031]** This arrangement is not free of critical aspects, which are clearly pointed out in Figure 8. Another feature of this arrangement of the select transistors is the fragmentation in a plurality of diffusion islands, as well as the need to form poly lines (the gate structures of the select transistors) in a relatively tortuous layout in order to create, on alternately either side, the necessary space for realizing the contacts.

**[0032]** Figure 9 shows a layout according to the present invention which also takes advantage of a second metal level thus allowing an interleaved arrangement of bitlines, as clearly illustrated in this figure.

**[0033]** For the same bunch of 32 bitlines, the layout according to the present invention, allows in the first place to form continuous diffusions, as opposed to the fragmented, ones of the prior art layout and makes possible a much more relaxed spacing, the realization of straight poly strips, and a contacting that may be distributed in an uniform manner along the respective diffusions in order to minimize resistances while reducing also the capacitance toward the body region. These two latter factors contribute decisively in reducing time constants and increasing the speed of the operation of memory.

**[0034]** By referring now to the scheme of Figure 9, on each row or order are realized alternately a select transistor (select gate) and an isolating transistor (isolating gate), as depicted in the figure by tracing the profile of the bitline BL_0<0-15> with solid lines (second level metal) and that of the bitline BL_1<0-15> with "phantom" lines (first level metal). Therefore, the select transistors of the first 16 bitline BL_0<0-15> are realized along the back row or order (at the top of Figure 9); being their common output represented by the OUT_0 node, while the select transistors of the second 16 bitlines BL_1<0-15> are realized along the front row or order, being their common output represented by the OUT_1 node.

**[0035]** In order to facilitate comparison with the architecture of Figure 8, the texts or levels of Figure 9 single out the advantageous aspects of the architecture of the invention.

## Claims

1. A semiconductor memory device comprising an array or matrix of memory cells organized in rows and columns, respectively addressable through orthogonal wordlines and bitlines individually selectable through respective multiplexers and wherein the multiplexer module for a certain minimum number (<0-15>) . or bunch of columns (BL_0<0-15>, BL_1<0-15>,...) comprises an identical number (<0-15>) of select transistors, the current terminals of each select transistor being coupled to one of said bitline and to a common output node (OUT_0, OUT_1), respectively, and
**characterized in that**
each multiplexer module for said minimum number of columns (<0-15>) is realized in a continuous strip in a space opposite to the terminals of two of said minimum number or bunches of columns (BL_0<0-15>, BL_1<0-15>), the respective bitlines of one bunch being interleaved with the respective bitlines of the other, and the two multiplexer modules being realized along two parallel strips; and **in that** it comprises
an isolating transistor having its own current terminals respectively coinciding with the coupling node of the current terminal of a first select transistor to the respective bitline and with the coupling node of another select transistor, adjacent to said first select transistor, to the respective bitline and a control terminal coupled to a source of a turn-off voltage of said isolating transistor.

2. The device according to claim 1, **characterized in that** the active areas of said adjacent select transistors are contiguous.

3. The device according to claim 1, **characterized in**

**that** the isolation amongst the respective diffusions of said transistors formed within the respective contiguous active areas is constituted by a channel region topped by a gate structure of said isolating transistor.

4. The memory device according to any of the preceding claims, **characterized in that** it utilizes a two level metal and in which two bunches of bitlines are interleaved, said select transistors relative to the columns of a first bunch of bitlines being arranged along a first row or order, alternately to said isolating transistors and said select transistors relative to the columns of the other bunch of bitlines being arranged along a second row or order, alternately to said isolating transistors, and wherein two orders of mutually interleaved of straight strips of polysilicon realize common gate structures of a select transistor of the first order or of a select transistor of the second order and respectively of an isolating transistor of first order or of an isolating transistor of the second order.

**Patentansprüche**

1. Halbleiterspeichervorrichtung, die eine Anordnung oder Matrix aus Speicherzellen umfasst, die in Zeilen und Spalten organisiert sind und jeweils über zueinander senkrechte Wortleitungen und Bitleitungen adressierbar sind, die einzeln über jeweilige Multiplexer auswählbar sind, wobei das Multiplexermodul für eine bestimmte minimale Anzahl (<0-15>) oder ein bestimmtes Bündel von Spalten (BL_0<0-15>, BL_1<0-15>, ...) die gleiche Anzahl (<0-15>) von Auswahltransistoren umfasst, wobei die Stromanschlüsse jedes Auswahltransistors mit einer der Bitleitungen bzw. mit einem gemeinsamen Ausgangsknoten (OUT_0, OUT_1) gekoppelt sind, und **dadurch gekennzeichnet, dass**
jedes Multiplexermodul für die minimale Anzahl von Spalten (<0-15>) in einem ununterbrochenen Streifen in einem Raum gegenüber den Anschlüssen von zwei der minimalen Anzahl oder der Bündel von Spalten (BL_0 <0-15>, BL_1 <0-15>) verwirklicht ist, wobei die jeweiligen Bitleitungen eines Bündels mit entsprechenden Bitleitungen des anderen verschachtelt sind, und die beiden Multiplexermodule längs zweier paralleler Streifen verwirklicht sind; und dass sie umfasst:

einen Isoliertransistor, der seine eigenen Stromanschlüsse, die mit dem Kopplungsknoten des Stromanschlusses eines ersten Auswahltransistors an der entsprechenden Bitleitung bzw. mit dem Kopplungsknoten eines weiteren, an . den ersten Auswahltransistor angrenzenden Auswahltransistors an der entsprechenden Bitleitung übereinstimmen, sowie einen Steueranschluss, der mit einer Quelle einer Abschaltspannung des Isoliertransistors gekoppelt ist, besitzt.

2. Vorrichtung nach Anspruch 1, **dadurch gekennzeichnet, dass** die aktiven Bereiche der benachbarten Auswahltransistoren nebeneinander liegen.

3. Vorrichtung nach Anspruch 1, **dadurch gekennzeichnet, dass** die Isolation zwischen den jeweiligen Diffusionsgebieten der Transistoren, die in entsprechenden nebeneinander liegenden aktiven Bereichen gebildet sind, durch einen Kanalbereich gebildet ist, auf dem eine Gate-Struktur des isolierenden Transistors angeordnet ist.

4. Speichervorrichtung nach einem der vorhergehenden Ansprüche, **dadurch gekennzeichnet, dass** sie ein Zweiebenenmetall verwendet und zwei Bündel von Bitleitungen verschachtelt sind, wobei die Auswahltransistoren für die Spalten eines ersten Bündels von Bitleitungen längs einer ersten Zeile oder Folge abwechselnd mit den Isoliertransistoren angeordnet sind und die Auswahltransistoren für die Spalten des anderen Bündels von Bitleitungen längs einer zweiten Reihe oder Folge abwechselnd mit den Isoliertransistoren angeordnet sind und wobei zwei Folgen von zueinander verschachtelten geraden Streifen aus Polysilicium gemeinsame Gate-Strukturen eines Auswahltransistors der ersten Folge oder eines Auswahltransistors der zweiten Folge bzw. eines Isoliertransistors der ersten Folge oder eines Isoliertransistors der zweiten Folge bilden.

**Revendications**

1. Dispositif mémoire à semiconducteur comprenant un réseau ou matrice de cellules mémoire organisées en rangées et en colonnes, respectivement adressables par des lignes de mot et des lignes de bit orthogonales sélectionnables individuellement par des multiplexeurs respectifs, et dans lequel le module multiplexeur pour un certain nombre minimum (<0-15>) ou groupe de colonnes (BL_0<0-15>, BL_1<0-15>,...) comprend un nombre identique (<0-15>) de transistors de sélection, les bornes de courant de chaque transistor de sélection étant couplées à l'une des lignes de bit et à un noeud de sortie commun (OUT_0, OUT_1), respectivement, et **caractérisé en ce que** :

chaque module multiplexeur pour le nombre minimum de colonnes (<0-15>) est réalisé selon une bande continue dans un espace opposé aux bornes de deux dudit nombre minimum

ou groupes de colonnes (BL_0<0-15>, BL_1<0-15>,...), les lignes de bits respectives d'un premier groupe étant entrelacées avec les lignes de bits respectives de l'autre, et les deux modules multiplexeurs étant réalisés selon deux bandes parallèles ; et **en ce qu**'il comprend :

un transistor d'isolement ayant ses propres bornes de courant coïncidant respectivement avec le noeud de couplage de la borne de courant d'un premier transistor de sélection vers la ligne de bit respective et avec le noeud de couplage d'un autre transistor de sélection, adjacent au premier transistor de sélection, vers la ligne de bit respective et une borne de commande couplée à une source d'une tension de coupure du transistor d'isolement.

2. Dispositif selon la revendication 1, **caractérisé en ce que** les zones actives des transistors de sélection adjacents sont contiguës.

3. Dispositif selon la revendication 1, **caractérisé en ce que** l'isolement entre les diffusions respectives des transistors formés dans des zones actives contiguës respectives est constitué d'une région de canal surmontée d'une structure de grille du transistor d'isolement.

4. Dispositif mémoire selon l'une quelconque des revendications précédentes, **caractérisé en ce qu**'il utilise un double niveau de métal et dans lequel deux groupes de lignes de bit sont entrelacés, les transistors de sélection relatifs aux colonnes d'un premier groupe de lignes de bit étant agencés selon une première rangée ou ordre, alternés avec les transistors d'isolement et les transistors de sélection par rapport aux colonnes de l'autre groupe de lignes de bit agencées selon une seconde rangée ou ordre, alternés avec les transistors d'isolement, et dans lequel deux ordres de bandes droites mutuellement entrelacées de silicium polycristallin réalisent des structures de grille communes d'un transistor de sélection du premier ordre ou d'un transistor de sélection du second ordre, et respectivement d'un transistor d'isolement du premier ordre ou d'un transistor d'isolement du second ordre.

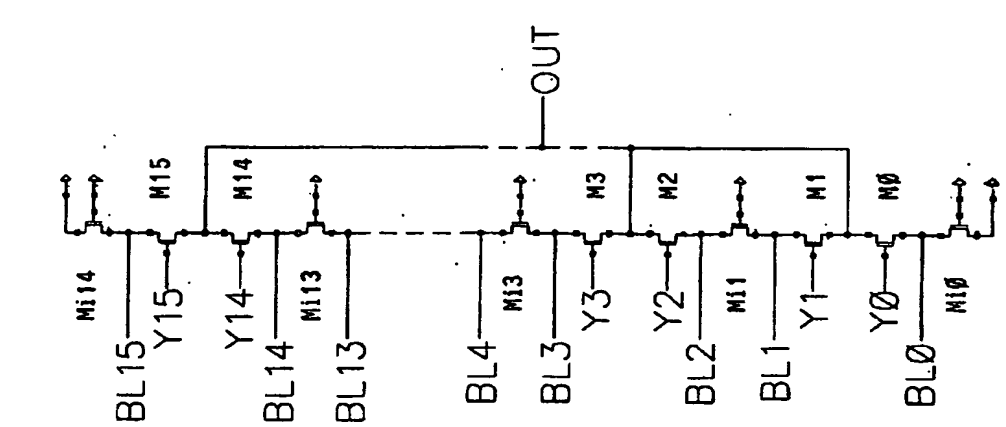


FIG. 3

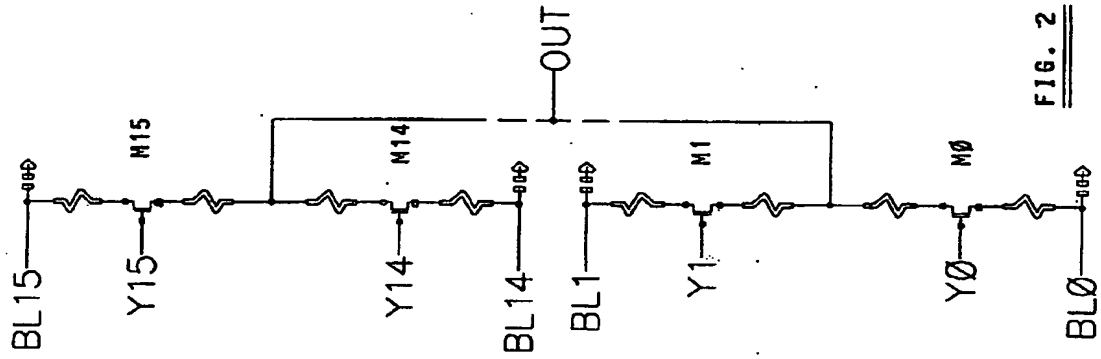


FIG. 2

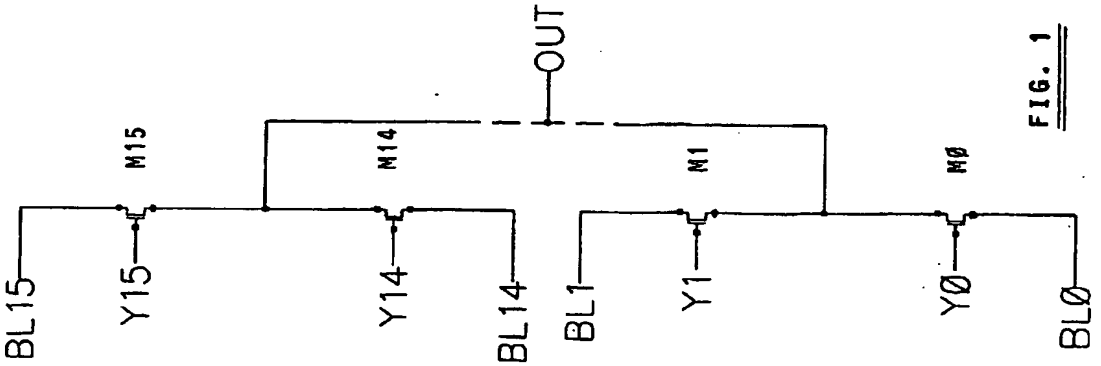


FIG. 1

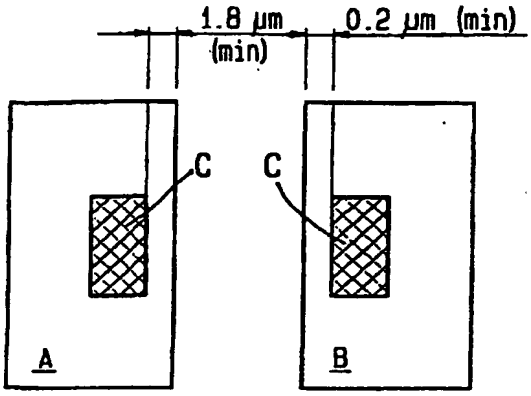


FIG.4

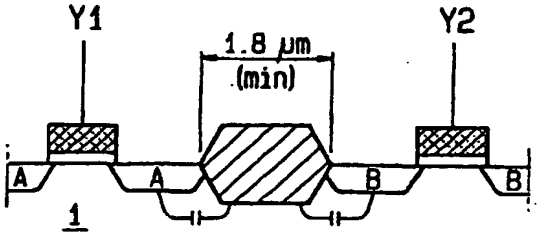


FIG.5

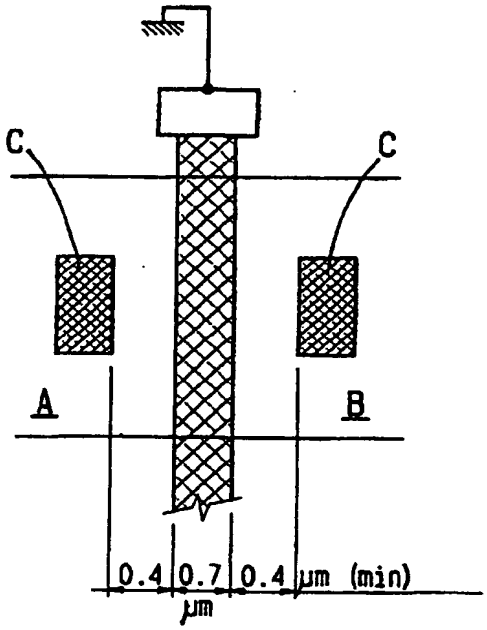


FIG.6

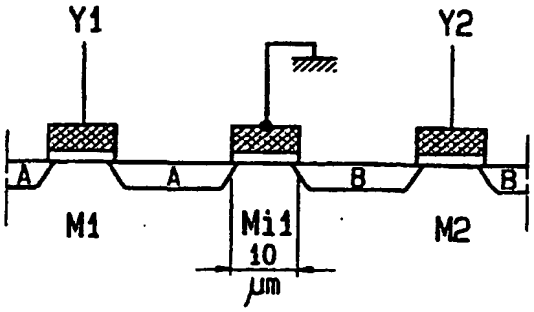


FIG.7

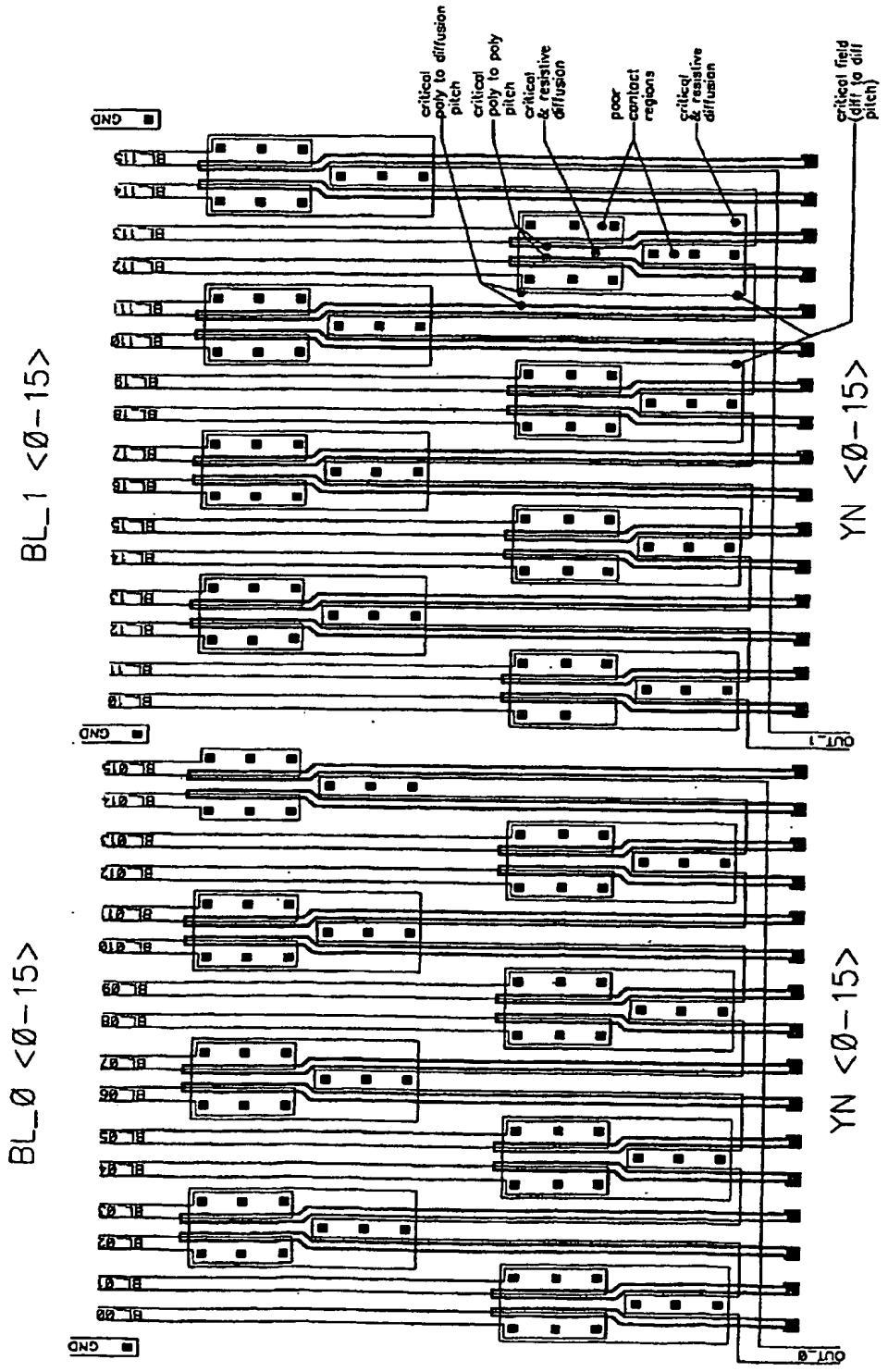
critical poly to diffusion pitch
critical poly to poly pitch
critical & resistive diffusion
poor contact regions
critical & resistive diffusion
critical field (diff to diff pitch)
BL_1 <0-15>
YN <0-15>
BL_0 <0-15>
YN <0-15>
GND
OUT_1
OUT_0

FIG. 8

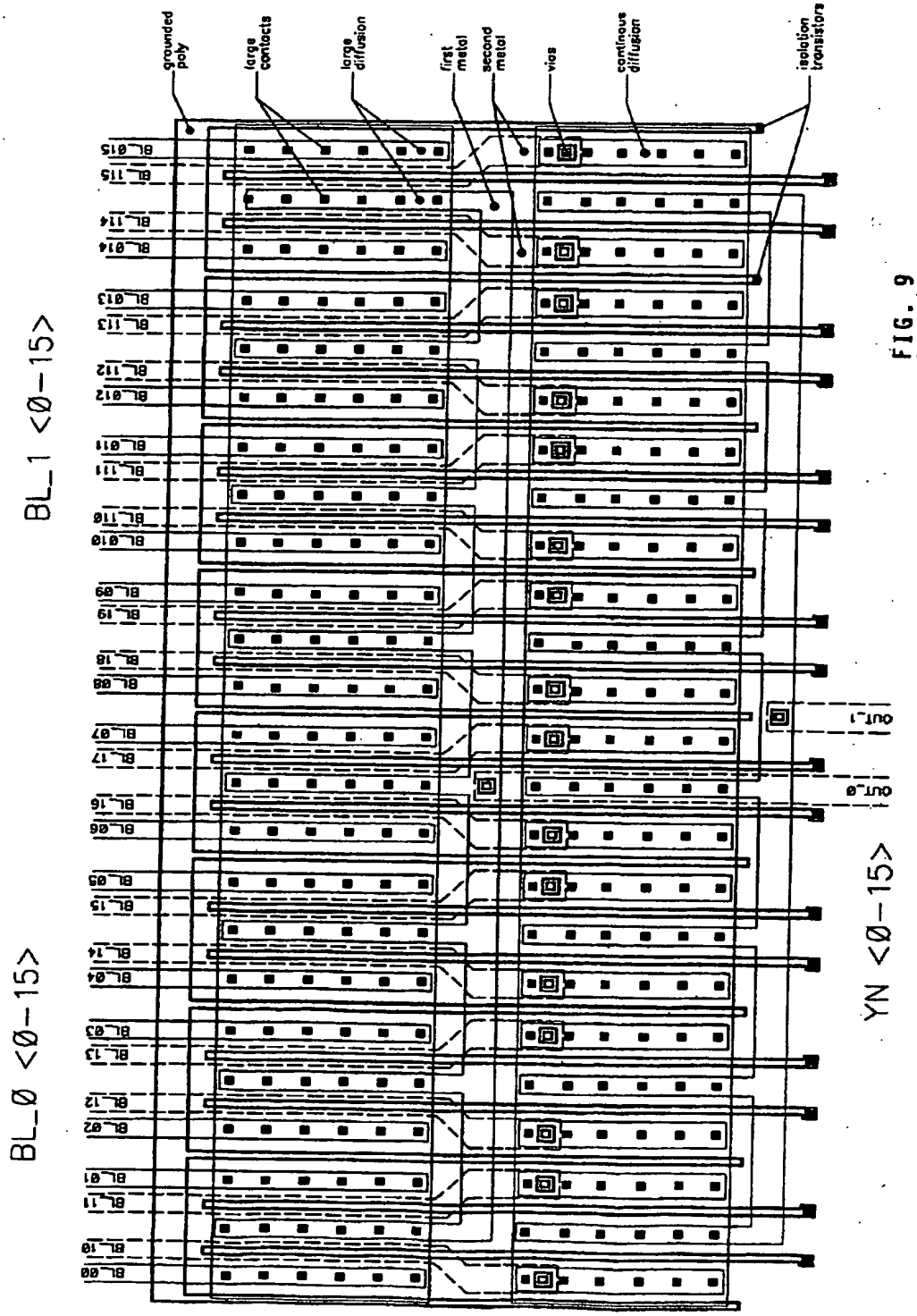
grounded poly
large contacts
large diffusion
first metal
second metal
vias
continous diffusion
isolation transistors
BL_1 <0-15>
BL_0 <0-15>
YN <0-15>
OUT_1
OUT_0

FIG. 9